A 1.4–2.7-GHz Analog MMIC Vector Modulator for a Crossbar Beamforming Network

Jesús Grajal, Javier Gismero, Mustapha Mahfoudi, and Felix A. Petz

***Abstract*—The design and performance of a monolithic 1.4–2.7-GHz vector modulator with analog amplitude and phase control are presented in this paper. A full 360° coverage range and a dynamic range greater than 13 dB is achieved by combining two out of three vectors 120°apart with variable amplitude. Amplitude control is performed by three sets of quasi-dual-gate MESFET's (two single-gate MESFET's in cascade) while the 120° shift among the vectors is achieved through *LC* filters covering the 1.4–2.7-GHz band. Since the active devices throughout the circuit are not working in saturation, large-signal models must be used in the simulations. The circuit is used as the matrix node element in an analog crossbar beamforming network (CBFN) and as the general-purpose wide-band vector modulator device.**

***Index Terms*—Beamforming network, MMIC, vector modulator.**

I. Introduction

PHASED-ARRAY antennas using gallium arsenide (GaAs) monolithic microwave integrated circuits (MMIC's) as control modules are gaining added significance for on-board satellite applications because of their ability to form multiple beams and to provide power sharing among beams. These active antennas offer improved operational flexibility by providing independent beam reconfigurability and steerability, resulting in more efficient use of satellite-power resources. In addition, with the generation of narrow beams, higher effective isotropic radiated power (EIRP) can be achieved, enabling direct communication with small earth stations, [1], [2].

A very important consideration in selecting the beamforming architecture is the kind of the array and the beamforming function implementation. Orthogonal beamforming based on crossbar arrangements is a well-known technique particularly efficient when the matrix elements are designed to control the relative phase and amplitude by command. These kinds of matrix elements require circuits providing both amplitude and phase control. These control circuits must be of small size, lightweight, of low power consumption, and reproducible. All these features can be optimized by using MMIC-based modules.

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Generally beamforming networks (BFN's) can be divided into three general categories: *purely digital* [3], [4], *mixed analog-digital* [5], and *purely analog* [6]. Typical MMIC-based modules comprise different individual circuits to perform the amplitude and phase-control tasks: variable phase shifters, variable gain/attenuation stages, and switches. This approach results in higher insertion losses (IL's) and cumulative errors, larger size, and a more complicated housing than using a single MMIC circuit. In addition, typical BFN architectures normally require power splitters/combiners increasing the overall size, weight, and complexity even more.

In this paper, an analog single-MMIC approach is presented. A dynamic range greater than 13 dB over a full 360° phase range in the 1.4–2.7-GHz bandwidth is obtained by combining the signal from two out of three vectors (each vector 120° phase shifted) with the adequate amplitude. In Section II, the general structure of the crossbar BFN (CBFN), which imposes the design requirements for the circuit, is analyzed to describe the real application environment for the circuit. In Section III, the detailed circuit-design approach is discussed, focusing on the amplitude control stage and filter design. Section IV presents the measurement and calibration procedures. The aim is to analyze the manufactured wafers in order to select the more than 100 MMIC components required for the CBFN unit. Results presented in Section V about performance of the circuit demonstrate the validity of the circuit design for a CBFN matrix based on a single MMIC device. Section VI summarizes the conclusions to be drawn from this paper.

II. CBFN Architecture: Impacts on the MMIC Module

The BFN is composed of a set of matrix control elements interconnected by transmission lines arranged in a crossbar architecture, as shown in Fig. 1. The input transmission lines feed the matrix elements and the output lines collect the signals processed by the nodes for delivery to the radiating elements. Ideally, the control node consists of an ideal voltage controlled-current source (i.e., $R_i = 0$, $R_o = \infty$, $C_i = C_o = 0$ in Fig. 1). In this case, the control node acts as an element which samples the input voltage signal delivering current to the output line.

The main characteristics of these ideal matrix elements are: 1) the amplitude and phase of the transconductance are controlled externally by means of command signals (control voltages); 2) the node component does not load the transmission lines, thus it has infinite input and output impedances, it is of low IL's, which depends on the transconductance of the control node; and 3) g_m) and the characteristic impedances of

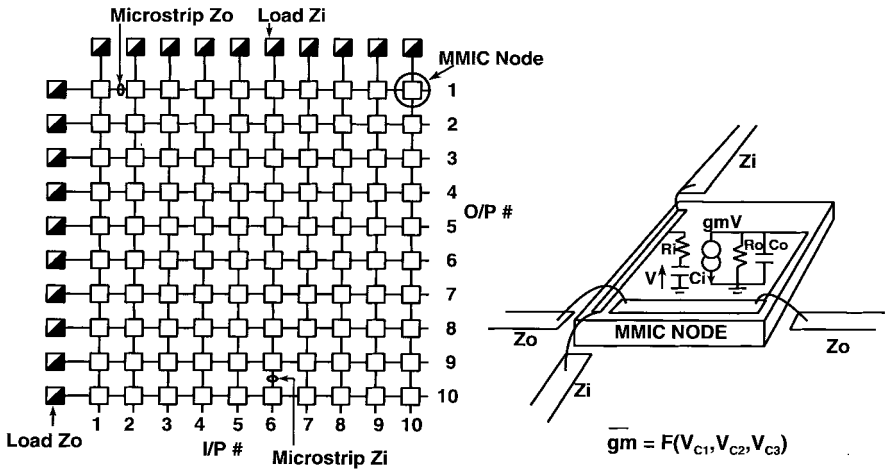


Fig. 1. CBFN architecture and control-node equivalent circuit.

input and output transmission lines (Z_i, Z_o. The power gain of such a node can be defined as

$$G = 10 \log \left(\frac{g_m^2 Z_i Z_o}{4} \right). \quad (1)$$

Strictly speaking, this gain should be increased in $10 \cdot \log(N)$, with N being the number of nodes fed by an input. The ideal control node can also be represented in terms of a Y-parameter matrix as

$$[Y] = \begin{bmatrix} 0 & 0 \\ g_m e^{j\theta} & 0 \end{bmatrix} \quad (2)$$

where both g_m and θ are externally controlled. However, the matrix element that has been implemented in GaAs MMIC technology does not perfectly match the characteristics of the ideal node. The input impedance can be represented as a series *RC* network (R_i, C_i) while the output impedance is best described as a parallel *RC* network (R_o, C_o). These parasitics will load the transmission lines, degrading the input and output VSWR and affecting the overall matrix performance by causing unbalance among different nodes due to the ohmic losses.

The reactive part of the input and output impedances are usually of capacitive nature due to the inherent capacitive effects of active MESFET devices. To get high impedance it is necessary to obtain small capacitances. But in any case, the reactive part of these impedances can be compensated with artificial transmission lines—a lumped inductance inside the MMIC or a short-length high-impedance transmission line (inside or outside the MMIC) together with the bonding wires and the capacitance of the circuit [7]. Of course, this method for the compensation of the capacitive effect of the circuit is limited by the value of the capacitance—high capacitor values imply high values of inductance for a given characteristic line impedance reducing the bandwidth of the artificial transmission line. On the other hand, reducing the characteristic line impedance results in a loss of power gain. Consequently, there must exist a tradeoff between the frequency band and the power gain. Fig. 2(a) shows the input matching in the matrix ports as a function of input resistance R_i for $Z_i = 40$, $C_i = 1.0$ pF, $L = 1.5$ nH. Fig. 2(b) shows the output matching as a function of output resistance R_o for $Z_o = 50$, $C_o = 0.2$ pF, $L = 0.5$ nH.

TABLE I
SYSTEM PERFORMANCES

Frequency Range	1.4-2.7 GHz (instantaneous bandwidth: 40MHz)
Maximum I. L. (per node)	20 dB (including unbalance)
VSWR (I/O)	< 1.5
Amplitude Control Range	13 dB, 5 bit resolution, accuracy better than ½ LSB
Phase Control Range	360°, 5 bit resolution, accuracy better than ½ LSB
Power Consumption	< 150 mW (per node)

Fig. 3 shows the effect of the resistive part of the input and output impedances on the CBFN matrix transmission unbalance—S_{21} parameters for the minimum distance between the input and output (best case), upper traces, and the maximum distance between the input and output (worst case).

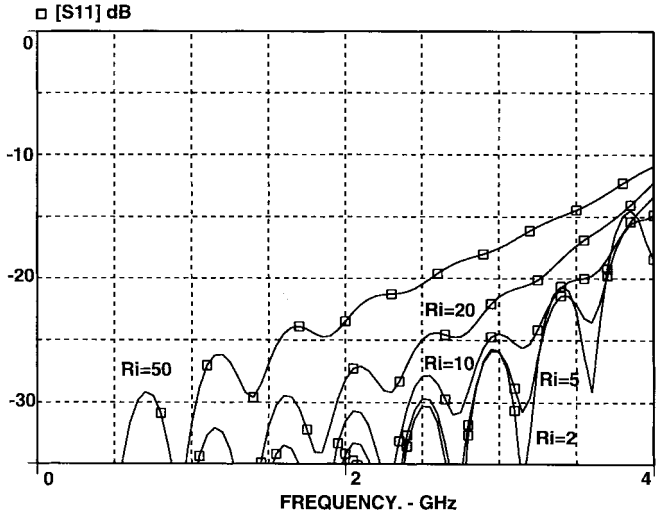
Figs. 2 and 3 show the limiting requirements for R_i, R_o coming from the unbalance analysis and not from the input/output mismatching.

A MESFET in common-source configuration offers an inherent high input impedance, supposing the input capacitance is embedded within an artificial delay line, as well as high transconductance. A MESFET in common-gate configuration will produce a very high resistive output impedance avoiding the need for an artificial transmission line due to the very low output capacitance in this configuration.

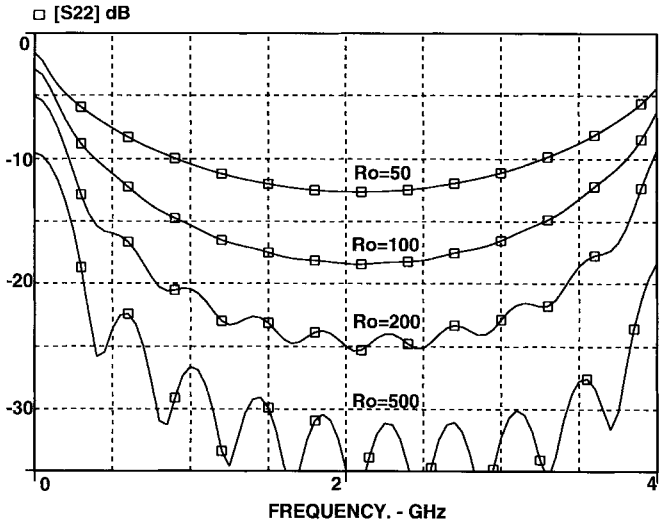
The CBFN system performances to be achieved are summarized in Table I.

The following electrical parameter values guarantee the IL and matching requirements with a maximum unbalance of 3 dB:

Transconductance g_m (maximum)	7 mS;
Input Resistance	$<2\ \Omega$;
Output Resistance	$>1200\ \Omega$;
Input/Output Capacitance	To be minimized to ease the artificial line design (<1.2 pF);
Z_i, Z_o	40, 50 Ω.



(a)



(b)

Fig. 2. (a) Effect of the input resistance of the node on the matrix input matching and (b) of the output resistance of the node on the matrix output matching.

III. Design Approach

The vector modulator developed configures three stages as follows.

1) The first stage performs the amplitude control via three dc control voltages.
2) The second stage is a set of three filters providing consecutive phase shifts of 120° in the band of interest.
3) The third stage is a combiner, which adds the three signals and generates a high resistive-output impedance.

A schematic diagram of the circuit is depicted in Fig. 4. The different stages are described in detail below. All the simulations have been performed using Series-IV software by HP-EEsof, with MESFET's simulated using the implemented Libra Curtice Cubic model with foundry-supplied parameters.

A. Voltage-Controlled Amplitude Stage

This is the input stage in the schematic diagram shown in Fig. 4, consisting of three sets of common-source MESFET's

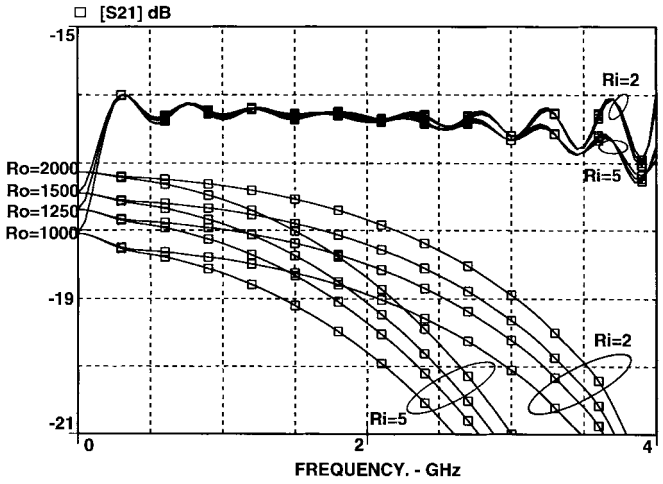


Fig. 3. Effect of the resistive part of the input/output impedance on unbalance.

($T1$) with active loads. The transconductance magnitude control is achieved by varying the MESFET $T1$ drain–source voltage $V_{\rm ds1}$ within the resistive region of its I–V characteristics. Gate–source voltage $V_{\rm gs1}$ selects the I–V characteristic while $T2$ gate voltage (control voltage) allows the effective bias point to move through its linear zone (see Fig. 5) where the transconductance is nearly proportional to the $V_{\rm ds1}$ voltage [8]

$$g_m = (A_1+2A_2V_{\rm gs}+3A_3V_{\rm gs}^2)\cdot\tanh(\gamma V_{\rm ds})\approx F(V_{\rm gs})\cdot\gamma V_{\rm ds} \tag{3}$$

neglecting the term which takes into account the pinchoff voltage increase with the drain–source voltage (it is supposed $\gamma V_{\rm ds}\rightarrow 0$).

$T1$ and $T2$ sizes are chosen to obtain the maximum transconductance and highest input impedance—opposite goals—with minimum dc power. On the other hand, special care has been taken to maintain the output impedance of this stage as constant as possible with respect to the control voltage in order to load the filter inputs with a constant impedance (strictly speaking, this impedance is constant only for low values of $V_{\rm ds}$).

Fig. 6 depicts the simulated and measured transconductance g_m of this stage versus the applied control voltage to the gate of $T2$ (66 μm), using the $T1$ (300 μm) gate–source voltage $V_{\rm gs1}$ as a parameter. Figs. 7 and 8 show the corresponding current consumption for a +3.5-V supply V_{DD} and the output impedance, respectively.

By studying these graphs the following observations can be made.

- When $T1$ is biased at high negative $V_{\rm gs1}$, higher transconductance values are possible with lower current consumption, but with a nonlinear control behavior and large output impedance variations (a direct consequence of biasing the main MESFET near the knee of the I–V characteristic curves).
- Biasing $T1$ at low negative $V_{\rm gs1}$ increases the current consumption for a given transconductance, but with the benefits of low-output impedance variations and a more

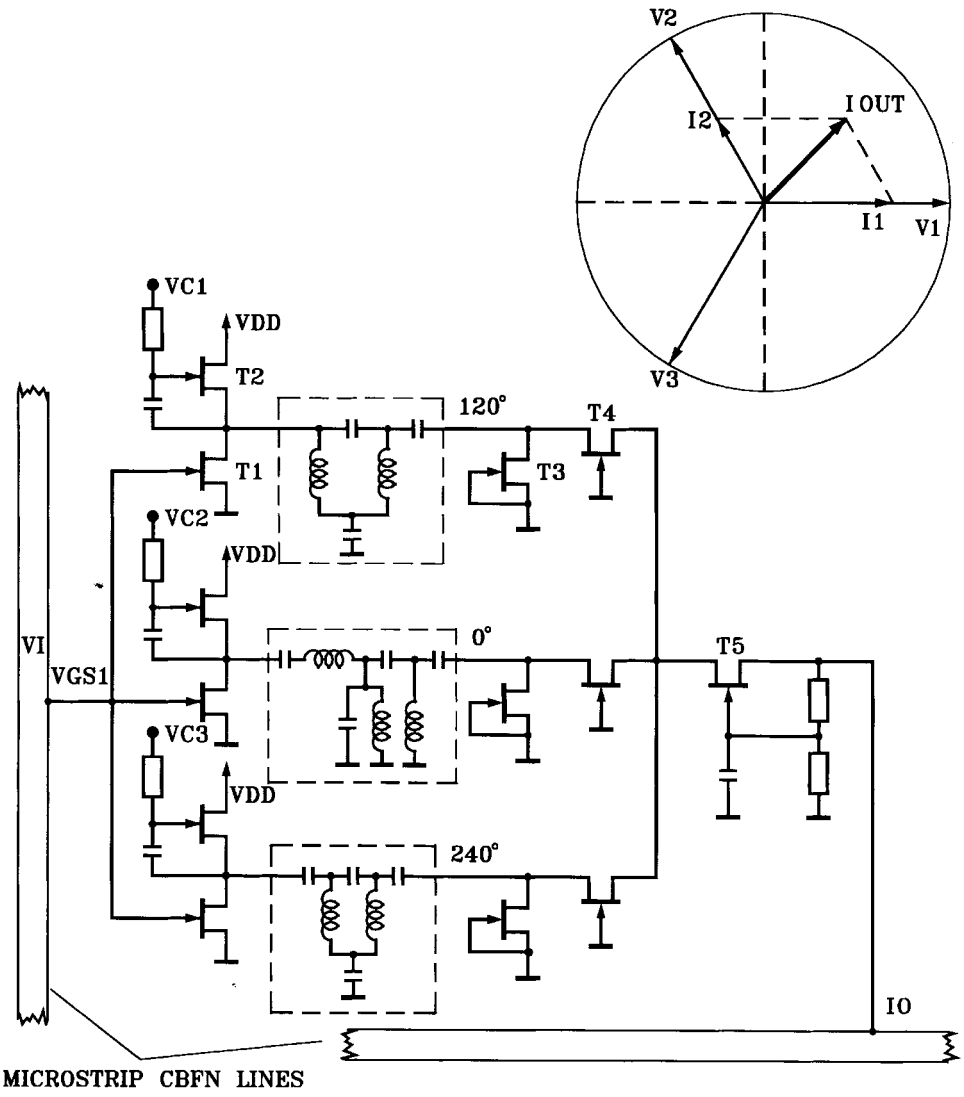


Fig. 4. MMIC schematic diagram.

linear behavior. In other words, the useful V_{ds} range is increased (see Fig. 5).

- For a control voltage V_c below -2 V, $T1$ is biased in $V_{ds1} = 0$ (off state). The fixed maximum operating point is $V_{ds1} = 0.5$ V corresponding to the control voltage $V_c = 0.5$ V. $T1$ gate–source voltage is chosen to $V_{gs1} = -0.8$ V. The first stage performances can be summarized as follows:

Maximum transconductance	22 mS;
Maximum current consumption	11 mA from a single $+3.5$ V supply;
Input impedance	$C_{in} = 0.35$ pF and $R_{in} = 4;\Omega$;
Output impedance	$R_{out} = 35$–$60\ \Omega$ and $C_{out} = 0.1$pF.

B. Three 120° Vectors Generation Stage

Because of the wide proliferation of MMIC analog I-Q vector modulators, a great deal of attention has been paid to the design and development of 90° vector generators. However, almost none of them can be applied to the 120° vector case, because they use structures with inherent antiphase properties.

In order to achieve low losses and good input/output matching, topologies which only comprise inductors and capacitors have been studied. Second-order all-pass filters have revealed to be the most suitable topologies due to their broad-band and small phase-shift error performances. The drawback is their balanced input and output nature, in fact, they are of lattice forms [9]. This problem can be overcome by transforming these balanced filters into grounded ones [10], obtaining structures like those shown in Fig. 9.

The network of Fig. 9(a) has been chosen for its smaller inductors value, which results in a smaller circuit size. Two all-pass filters with this configuration have been designed whose phase responses are 240° shifted from each other while the third filter is a bandpass one optimized to have the desired phase shift of ±120° and a similar amplitude response with respect to the other two filters. Fig. 10 shows the simulated amplitude response of the three filters predicting an unbalance lower than 1.5 dB. Fig. 11 shows the simulated phase behavior.

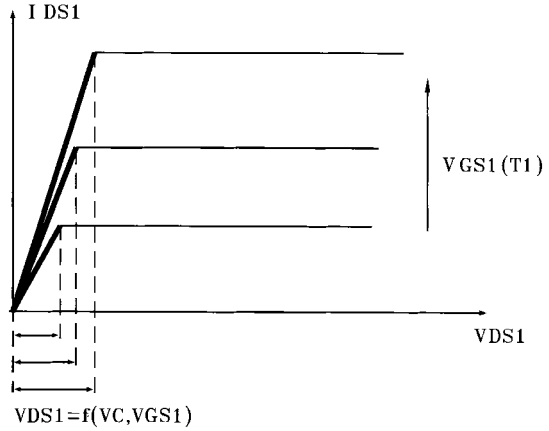


Fig. 5. Biasing range for $T1$.

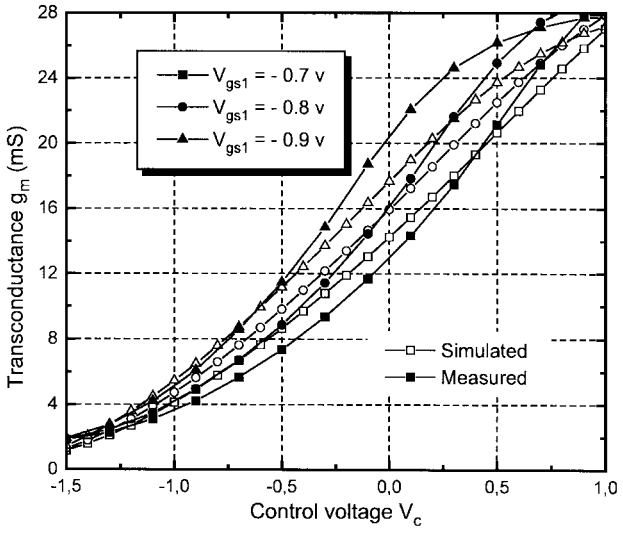


Fig. 6. Simulated and measured transconductance of first stage.

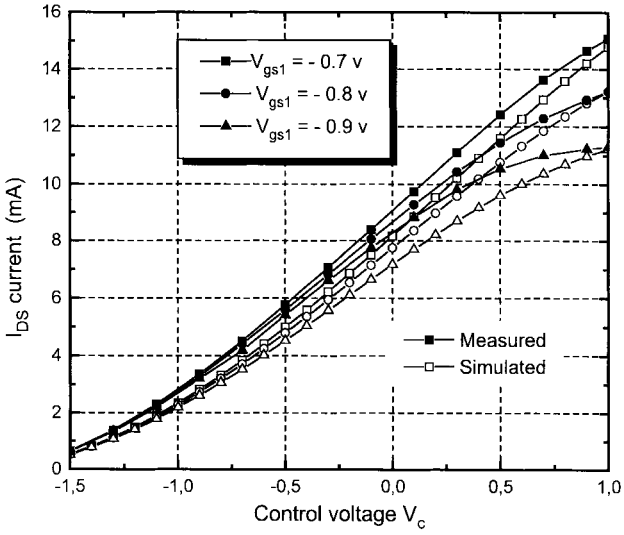


Fig. 7. Simulated and measured current consumption of first stage.

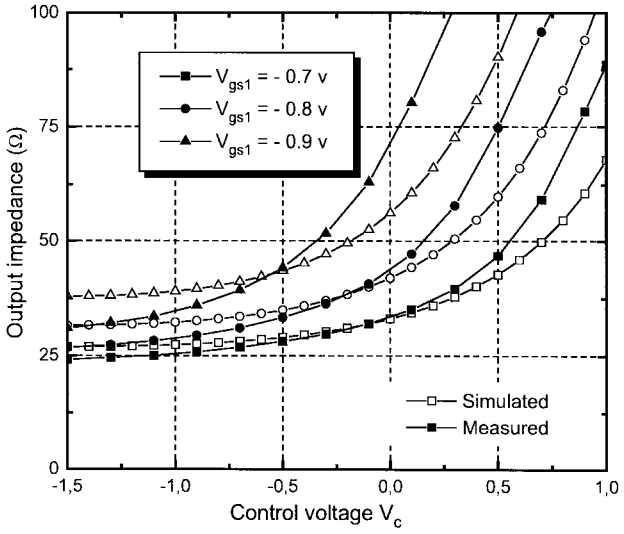


Fig. 8. Simulated and measured output impedance of first stage.

C. Output Stage

This stage acts as a three-way combiner, adding the three vectors generated in the previous stages and isolating the three paths. The configuration of this stage must achieve the following requirements: the input impedances must match the filter output impedance in each path and output impedance must be high enough to avoid loading the output transmission line.

The most appropriate configuration is a common-gate MESFET buffer. As can be deduced from Fig. 4, the input and output impedances of this stage are determined by internal parameters of the MESFET $T4$ (g_m, $R_{\rm ds}$) and by the output impedance of the filter (R_f):

$$Z_{\rm in} \approx \frac{1}{g_m} \approx R_f \tag{4}$$

$$Z_{\rm out} \approx R_f + R_{\rm ds} + g_m R_{\rm ds} R_f = R_f + 2R_{\rm ds}. \tag{5}$$

Of course, this is only the output impedance of one of the branches of the signal combiner, the common output impedance of the circuit is divided by three ($Z_{\rm out} \approx 200\ \Omega$). This output impedance obtained is unfortunately not high enough for the CBFN application, mainly because it is the cause of unbalance among different nodes (see Fig. 3). Therefore, a second stage in common-gate configuration is added to obtain the desired value ($Z_{\rm out} > 1200\ \Omega$). It is necessary to point out that the MESFET's in the output stage are not working in complete saturation since a single bias supply of only 3.5 V is used to bias the three devices ($T3$, $T4$, $T5$), and consequently the value for the output impedance is calculated using the large-signal models supplied by the foundry. The estimated current consumption of this stage is 20 mA.

The circuit was fabricated at GMMT (Caswell, U.K.) using the standard 0.5-μm MESFET F20 process. The MMIC chip layout of the circuit (2.3-mm side length) is shown in Fig. 12.

IV. Measurement and Calibration Algorithms

A. Screening

A total of 1200 circuits were processed (2 wafers) for the CBFN application. Previously, a series of 38 circuits was fabricated and measured as a part of a multiproject run to

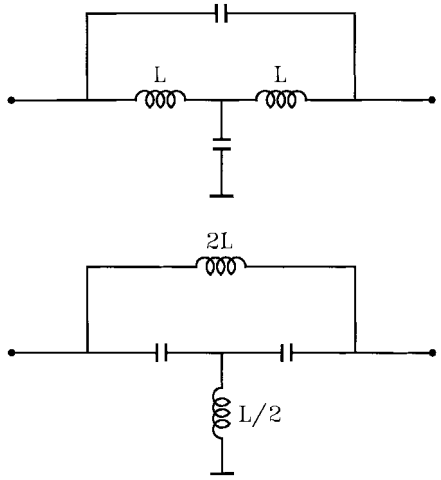


Fig. 9. All-pass filter structures.

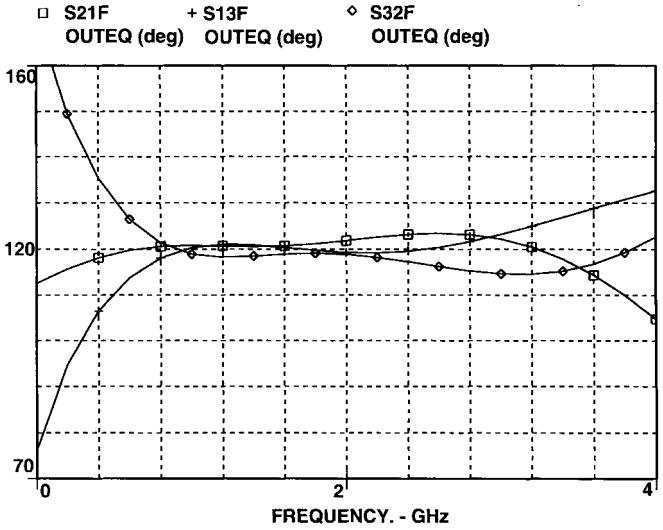


Fig. 11. Three filters simulated insertion phase difference.

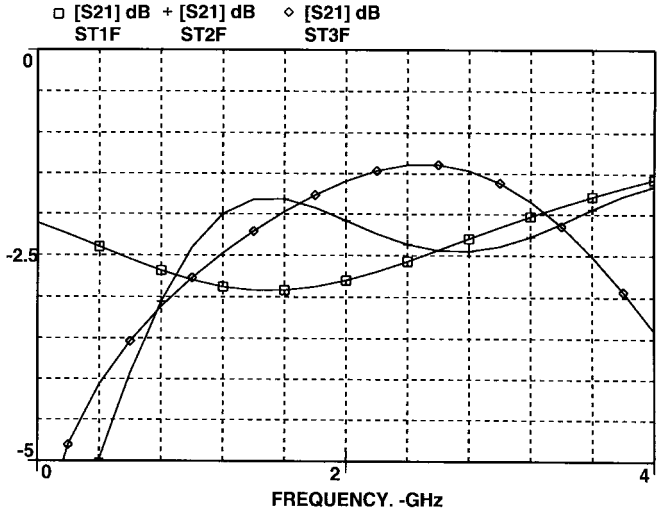


Fig. 10. Three filters simulated amplitude response.

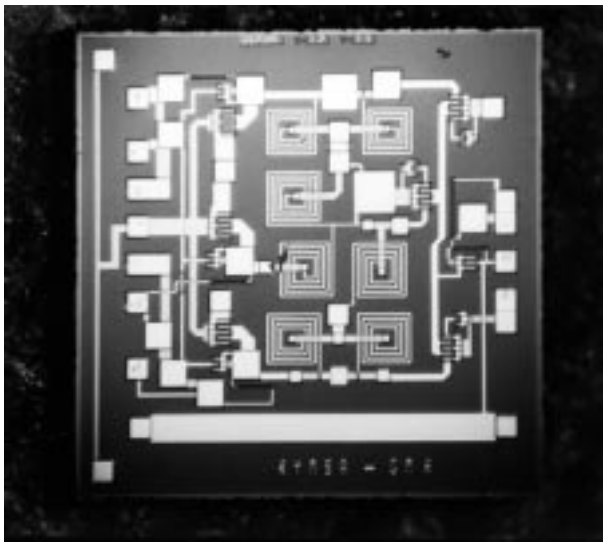


Fig. 12. Photograph of the circuit.

verify the validity of the design [11]. One of the conclusions drawn after the characterization of these first 38 circuits was the existing dispersion in the transmission parameter among the circuits along the wafer, being a result of both process variations—mainly pinchoff voltage, and the linear region where $T1$ devices are working and where these variations are more apparent. Thus, a fast and accurate characterization process became necessary to select the more than 120 circuits required for the application.

The first step of the screening process was carried out at the foundry facilities (GMMT) with on-wafer measurements of the circuit output-stage dc-current consumption (@ $V_{DD} = 3.5$ V, $V_{Ci} = -3$ V). Those circuits with deviations in excess of $\pm 20\%$ over the estimated one, in accordance with the large-signal model, were rejected. With these first dc measurements a total of 400 circuits were selected.

Within this set of circuits, a more selective screening was carried out by selecting those circuits with the closest responses in the quasi-Gaussian distributions for the S_{21} parameter. With this second criterion, a set of 180 circuits were selected for further extensive measurements, providing the final components to be included in the CBFN unit.

B. Measurements

As was previously stated, the three vectors comprising the amplitude modulator are isolated from each other, thus measurements of the individual vectors provide enough information to predict the circuit behavior for any combination of control voltages. This fact, verified through the measurements performed on the first 38 circuits, allows a reduction in the total number of RF measurements and simplifies the test setup.

The four S-parameters of the three single-signal vectors (i.e., only one active at a time, being the other two vectors switched off by $V_c < -2$ V) were measured at 21 bias points sweeping the control voltages V_{ci} from -1.5 to $+0.5$ V. The whole process takes approximately 20 min per chip and is controlled by the software Anacat from Eesof (controlling both

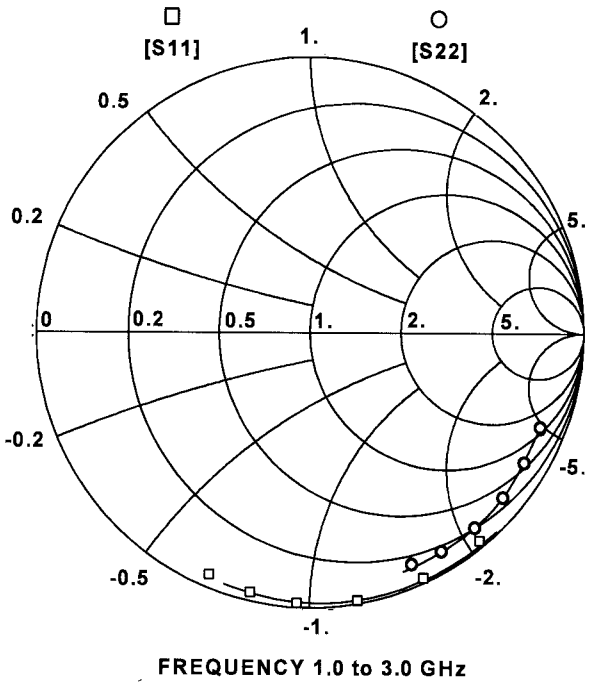


Fig. 13. Simulated (lines) and measured (dots) input and output impedances.

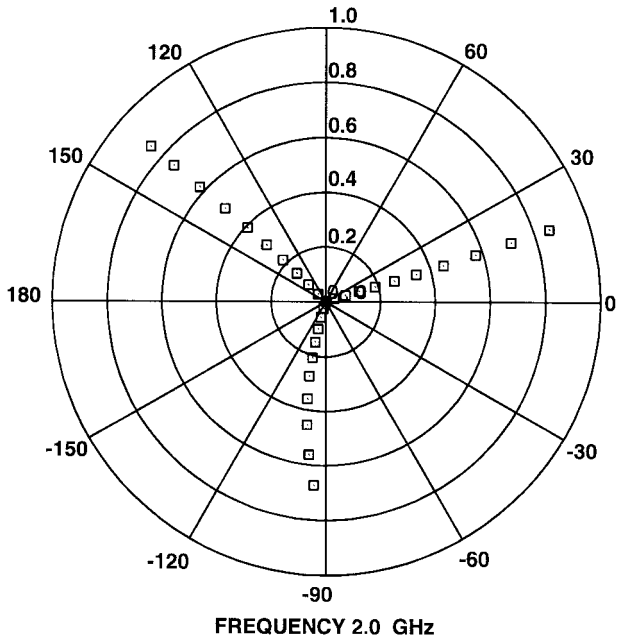


Fig. 14. Simulated response of the three primary vectors ($F = 2$ GHz).

the network analyzer (NWA) and the dc source–monitor); the measured data are sent to another computer for processing. It is important to mention that from circuit to circuit there are variations in the S_{21}-parameter (which will be overcome with a subsequent calibration process), but with respect to the other three parameters these variations are negligible, so it should be possible to reduce the mentioned measurement time by approximately 75% when measuring only the S_{21}-parameter.

C. Calibration

The calibration process begins with the interpolation of the measured S_{21} parameter (magnitude and phase) of the three single vectors as a function of the control voltage. Then, the required constellation is formed ($32 \cdot 32$ points, 5-b resolution both in phase and amplitude) within the dynamic range of 13 dB. The digital-to-analog converter (DAC) used in the control unit of the CBFN provides 80-V points in the range -1.5 to $+0.5$ V (8-b DAC, 256 points in the range -5–1.5 V, step 25 mV), so it is possible to obtain a $3 \cdot 80 \cdot 80$ points constellation. Finally, the best achievable points and associated control voltages for the three vectors are found as the closest ones in the latter constellation to the ideal ones in the desired constellation. Actually, there are only two active vectors at the time, so each state has an associated pair of control voltages. After the best match between achievable and ideal points is performed, the statistical analysis of errors is carried out. The algorithm also provides the pair of control voltages required to obtain any desired state in the magnitude–angle plane.

V. Results

For the simulations and measurements performed, the S-parameters of the stand-alone MMIC have been measured without embedding the component in an external microstrip environment (direct measurement using a microprobe station).

A. Input and Output Impedances

Fig. 13 shows the simulated and measured input and output impedance of the MMIC for a control voltage of $V_c = 0.5$ V. These results are nearly independent of the state being measured, as expected, and good agreement is observed with theoretical predictions except for the input capacitance that is a little bit higher than the simulated one (1.2 pF instead of 1 pF). This is probably due to the fact of having used a large-signal model well suited for the saturation zone, but not so well in the linear region where the dependences of $C_{\rm gs}$ and $C_{\rm gd}$ on both $V_{\rm gs}$ and $V_{\rm ds}$ are not correctly modeled.

The mean value for the input resistance is 2 Ω (for all chips, signal vectors, and control voltages) with a standard deviation lower than 0.5 Ω. The output resistance is well in excess of 1200 Ω and the output capacitance is below 0.12 pF. Of course, these values are obtained after de-embedding the circuit from the input and output sections of the microstrip line inside the chip. It can be seen in the layout of the circuit shown in Fig. 12 that the input line section (high characteristic impedance) is part of the input artificial line, while the line section at the output is simply a 50-Ω one.

B. Transmission Measurements

Fig. 14 shows the simulated response for the three primary vectors at 2 GHz when sweeping the control voltage from -1.5 to 0.5 V. In contrast, Fig. 15 displays the measured response for the whole set of chips (180 pieces). Similar results are obtained at other frequencies. A nearly constant insertion phase can be observed for two of the vectors; however, the third one shows a curvature (as simulated). This undesired effect is due to the higher sensibility of the corresponding

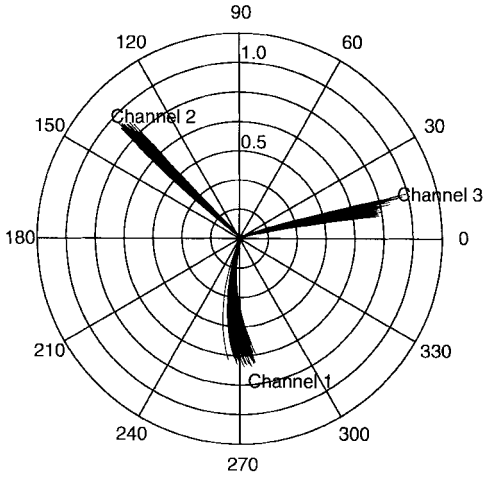


Fig. 15. Measured response of the three primary vectors ($F = 2$ GHz, 180 circuits).

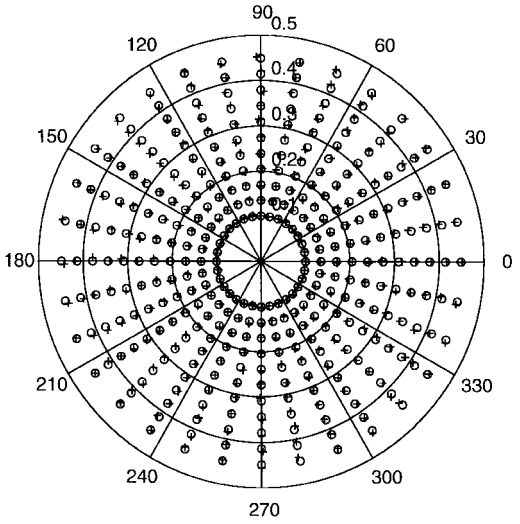


Fig. 17. Ideal and theoretically achievable constellations (2 GHz).

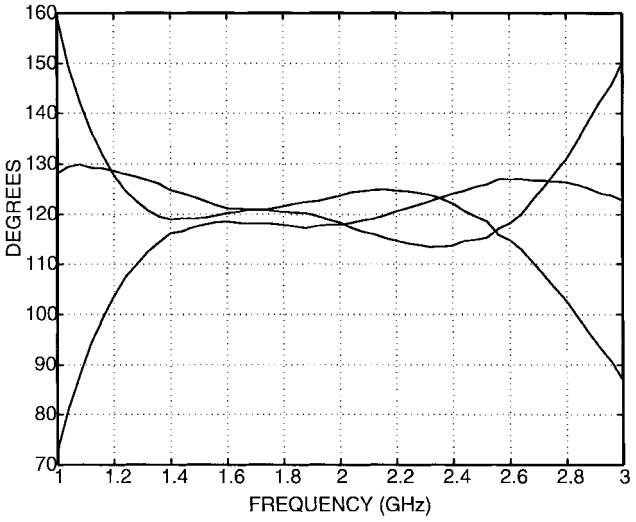


Fig. 16. Measured mean value of phase difference between vectors (180 circuits).

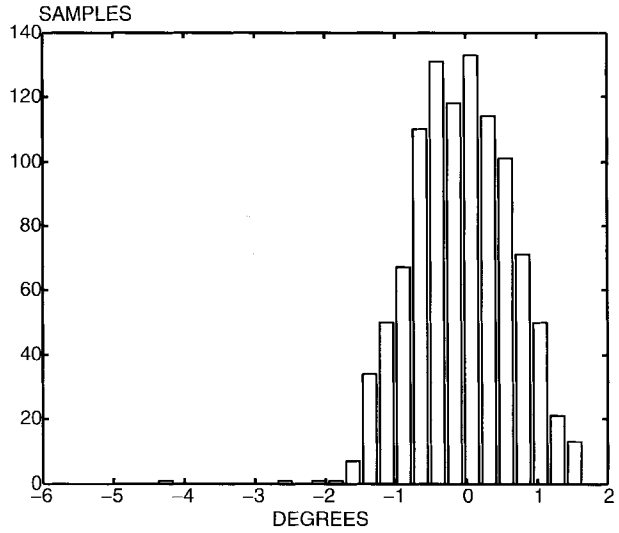


Fig. 18. Phase error distribution (degrees) for the $32 \cdot 32$ points constellation (2 GHz).

filter-insertion phase behavior to the variable output resistance of the first stage. The impact of this behavior is a reduction of the maximum achievable amplitude when combining this vector and another one (since phase errors are compensated by calibration). Anyway, for S_{21}-parameter amplitudes below 0.5 ($g_m = 5$ mS), phase error is below 7° in the whole band, as can be observed in Fig. 16 where the mean value for the phase difference between vectors for all the chips are shown for a control voltage of $V_c = 0$ V (mean $|S_{21}| = 0.5$).

C. Vector Modulator

In this section, the description and the results of the circuit working as the vector modulator are shown. Fig. 17 shows the ideal constellation (32×32 points, "o") and the theoretically achievable constellation (best points from among the possible $3 \times 67 \times 67$ points, "+") at 2 GHz. For the sake of clarity, only 11 points per phase are shown. Note that a step of 30 mV in the range −1.5–0.5 V (67 points) has been used in the simulations and measurements below, instead of the available step of 25 mV (meaning 42% less number of points). Figs. 18 and 19 show the phase and amplitude error distributions, respectively, for this theoretically achievable constellation.

TABLE II
MEAN AND STD ERROR VALUES FOR THE THEORETICALLY ACHIEVABLE CONSTELLATIONS

Freq. (GHz)	1.2	1.4	1.6	1.8	2.0	2.2	2.4	2.6	2.8
Mean Ampl. Error (dB)	0.48	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.1
Std Ampl. Error (dB)	1.28	0.12	0.12	0.11	0.12	0.11	0.12	0.11	0.2
Mean Phase Error (deg.)	0.0	0.0	0.0	0.0	-0.1	0.0	0.0	0.0	0.0
Std Phase Error (deg.)	4.0	0.74	0.67	0.75	0.7	0.74	0.76	0.65	0.7

Table II summarizes the mean and standard (STD) deviation values for the error distributions at different frequencies in the band.

To validate the calibration algorithm, a constellation of 48 points was measured at three frequencies in the band of

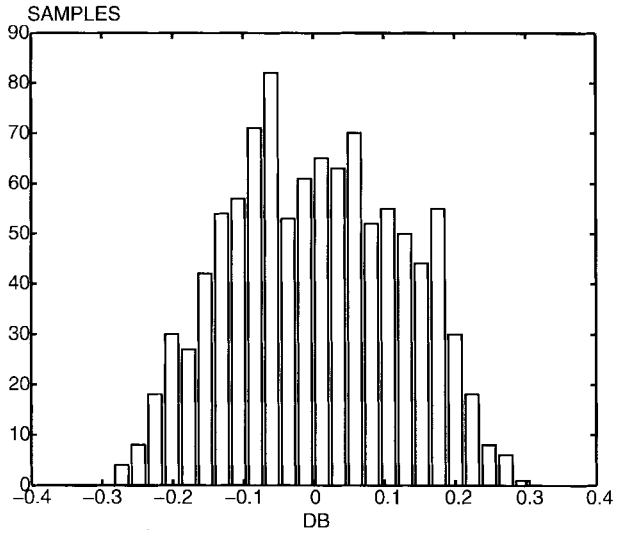


Fig. 19. Amplitude error distribution (dB) for the $32 \cdot 32$ points constellation (2 GHz).

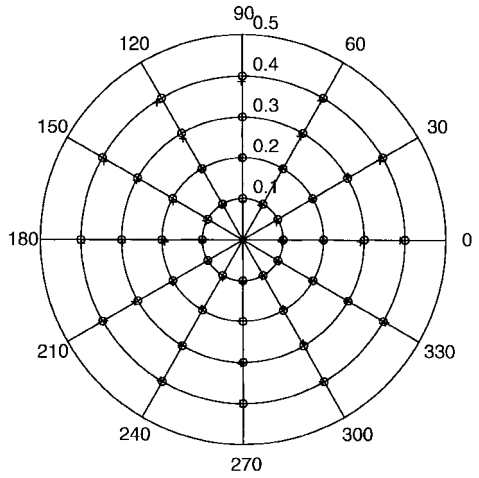


Fig. 20. Ideal (o) and measured ($+$) 48-point constellations at 2 GHz.

TABLE III
MEAN AND STD ERROR VALUES FOR THE MEASURED 48-POINT CONSTELLATIONS

Freq. (GHz)	1.6	2.0	2.4
Mean Ampl. Error (dB)	0.03	0.05	0.02
Std Ampl. Error (dB)	0.18	0.2	0.2
Mean Phase Error (deg.)	-0.1	-0.15	-0.1
Std Phase Error (deg.)	1.2	1.7	1.6

interest. Fig. 20 shows the theoretical (o) and measured (+) results at 2 GHz. Table III summarizes the mean and STD values for the error distributions at the three frequencies.

D. Power Consumption

The maximum power consumption of the first stage is 2×3.5 V $\times$ 11 mA (two vectors activated giving the highest amplitude). Output stage consumption is fixed to 3.5 V $\times$ 20 mA, which yields a maximum of 147 mW for the whole MMIC component. Of course, the mean power consumption will be lower than this value since most of the states do not require the combination of the highest amplitude vectors.

VI. CONCLUSIONS

An analog wide-band MMIC vector modulator using a three-vector approach has been presented. The circuit is well suited for BFN applications offering a full 360° phase range within a dynamic range in excess of 13 dB. The circuit uses a novel arrangement of two single-gate MESFET's to implement the variable gain stage and all-pass filters to obtain the desired phase shift among vectors. There is a good agreement between simulations and measurements, although the active devices are not operated in saturation for which the large-signal models have been extracted.

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